# Hemanth Kalaiyappan

**Thiruvallur, Tamil Nadu**

**DFT Engineer** | **VLSI Design-for-Test (DFT)** | Scan • ATPG • EDT/OCC • MBIST • Tessent

**Graduation: 2026**

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## Summary

- Final-year ECE student specializing in **Design-for-Test (DFT)** with hands-on experience using **Siemens Tessent** across scan, MBIST, EDT/OCC, and ATPG flows.
- Executed DFT implementation and ATPG activities on both **hierarchical** and **flat** designs up to **42K flip-flops**, including DRC cleanup, scan validation, coverage analysis, and pattern simulation.

## Skills

| | |
|---|---|
| **DFT** | Scan fundamentals, scan chains, **DFT DRC checks**, **scan stitching**, scan insertion, scan validation, **ATPG**, stuck-at/transition fault concepts, fault coverage analysis, **EDT compression**, **OCC**, **MBIST**, BSCAN/JTAG, IJTAG |
| **RTL/Digital** | Verilog, FSMs, clock/reset fundamentals, combinational and sequential logic |
| **Scripting** | TCL |
| **Programming** | C/C++ |
| **Tools** | Siemens Tessent, ModelSim/GTKWave, Cadence Genus/Virtuoso, Vivado, Yosys, Icarus Verilog, Linux, Git/GitHub |
| **Fault Models** | Stuck-at Fault, Transition Delay Fault, Fault Coverage Analysis |

## Industry Training — VLSIGURU (DFT using Siemens Tessent) 2025–Present

- Executed Tessent-aligned flow: **DFT DRC** • **Scan Insertion/Stitching** • **EDT/OCC** • **ATPG** • coverage review/debug.

## Projects

### Communication Chip — Full DFT Flow (Hierarchical Design)

*Tessent, Scan, MBIST, EDT/OCC, ATPG*

- Worked on a hierarchical design with parent core and multiple child cores (~**4K flip-flops**).
- Performed **MBIST insertion**, **scan stitching**, and **DFT DRC cleanup** using Siemens Tessent.
- Integrated **EDT compression** and **OCC insertion**; performed ATPG setup, fault coverage analysis, and DFT violation debug.

### Navigation Chip — Full DFT Flow (Flat Design)

*Tessent, Scan, MBIST, EDT/OCC, ATPG*

- Worked on a flat design with ~**42K flip-flops**.
- Executed **MBIST insertion**, **scan stitching**, **DFT DRC cleanup**, and **EDT/OCC** integration for compressed scan.
- Performed ATPG coverage analysis and DFT violation debug for fault coverage improvement.

### Secure Root-of-Trust Subsystem — Final Year Project

*SystemVerilog, UVM, APB, Multi-clock*

- Designed a multi-clock secure subsystem with **APB interface**, watchdog timer, and hardened FSM.
- Implemented resilience: **dual-rail FSM encoding**, **shadow registers**, **reset abuse detection**.
- Developed a complete UVM verification environment including sequences, driver, monitor, scoreboard, assertions, and functional coverage.
- Achieved **98.18% functional coverage** and **82/82 passing checks** across **19 verification scenarios**.
- **Paper Presentation:** Presented this project as a paper at a college-level conference.

## Education

### Sri Venkateswara College of Engineering (SVCE) 2022–2026

*B.E., Electronics and Communication Engineering | CGPA: 8.47*

Class XII (Math & CS), 73.2% — Maharishi International Residential School 2020–2022

Class X, 91.33% — ABS Vidhya Mandhir 2018–2020

## Certifications

NIELIT (RTL-to-GDSII) • NPTEL VLSI Design Flow • Verilog HDL Masterclass • SystemVerilog Essentials